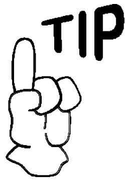
2. GETTING STARTED

2.1 AC LINE CONNECTION AND INITIAL SETUP

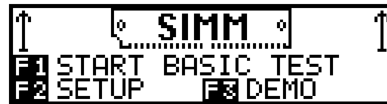
SIMCHECK II, or SIMCHECK II se, comes with a universal power supply, which can be use d in domestic or international markets. Connect the output plug of the enclosed AC adapter to the power jack at the rear of SIMCHECK II.

To activate SIMCHECK II, press the ON/OFF switch. When turned on, the **green** LED (power on) indicator is illuminated and the display shows the internal Power-On-Self-Test, the product copyright notices and the program version number, as in the following screen:

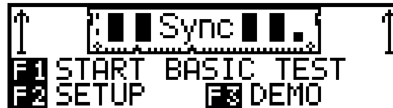


Experienced SIMCHECK users may wish to skip this section and move on to NOTES FOR SIMCHECK USERS in the next chapter.

The unit then stops at the STANDBY mode where you are prompted with the following message to insert a module and start the test:



SIMCHECK II automatically recognizes the adapters which are mounted on its Expansion Port. When an adapter is connected, such as the Sync DIMMCHECK 168 or the DRAM CARD ADAPTER, the STANDBY message will change to reflect the presence of the adapter after the first test:



2.2 THE DEMO MODE

The Demonstration program provides a detailed overview of SIMCHECK II's operation. It also familiarizes you with the display messages, graphics, and audible signals used by SIMCHECK II while a variety of faults are simulated.

- DO NOT INSERT A MODULE WHEN USING THE DEMO

PROGRAM - all display sequences are internally generated.

- The DEMO mode is initiated by pressing F3 in the STANDBY mode. The program is designed to be self-explanatory. Each screen is displayed for a preset amount of time.

- Press ↑ to accelerate the demo pace. Pressing F1 will restart the DEMO mode. If you would like to go back to a previous screen, you may press ←, or if you choose to add additional time to the current screen, you may press ↓.

- The DEMO mode incorporates portions of the actual program during which the keys function in a prescribed way corresponding to the currently demonstrated feature. During such demonstrations, you may need to either press the ESC key to move on, or simply elect to wait a few moments for the DEMO to continue on its own.

- At the end of the demonstration, SIMCHECK II returns to the STANDBY mode. You may leave the DEMO mode at any time by pressing ESC. It may be necessary to press ESC more than once to end the DEMO if it is during a demonstration feature.

After reviewing the demonstration, you should be familiar with SIMCHECK II's basic operation and capabilities.

2.3 OVERVIEW OF SIMCHECK II OPERATION

You start the test procedure by pressing F1 to initiate the BASIC test. Although it lasts only a few seconds, the BASIC test provides you with a lot of information on the module under test.

```
 BASIC TEST  AAAAAAAA
     BYTES: B1 ▲▲▲▲ B4
00:01.3    55/125nS  5V
16Mx32     FPM       B2
```

As shown above, SIMCHECK II is testing the module at the default voltage of 5V, identifies its size as being 16Mx32 and states that it operates in Fast Page Mode. The speed notation of 55/125nS indicates that the module has an access time of 55nS, and a cycle time of 125nS (Please refer to APPENDIX C for an explanation of Cycle Time Measurement). A dynamic graphic representation of the individual bytes and the HEX test patterns

is shown as the test progresses. Every memory cell of the DUT (Device Under Test) is fully tested several times to insure detection of all "stuck at" type failures. The BASIC TEST is followed by a few structure screens.

The BASIC TEST is sufficient for most of your memory testing needs, so you can press ESC to terminate the current test.

You may leave the module on for the next major test, the EXTENSIVE test, which gives you a more thorough and comprehensive procedure. This test lasts a few minutes depending upon module size.

Within the EXTENSIVE test are different individual test phases. The initial phase is Voltage Cycling, which uses varying patterns on the DUT, while the voltage is applied at different levels from 4.50V through 5.50V (or 3.0V to 3.6V). The MODE Analysis test follows, giving information on the detection of FAST PAGE or EDO MODE, as well as other DRAM modes of operation. Next is the Voltage Bounce test which repeatedly reads and writes to the module while the voltage is bounced from the upper and lower extremes. The MARCH UP/DOWN test then begins testing for adjacent cell interference, using data patterns that are more likely to reveal such a problem. Following are the two comparative test phases: Relative Refresh and Relative Spikes. Relative Refresh tests for data retention between refresh cycles. The figure given is only for comparative measurements, and is not an absolute value, that is, a chip having a relative value of '5' retained data integrity twice as that with a value of '4'. The Relative Spikes test phase performs a data retention test while the module is subjected to various sizes of voltage spikes. The next phase in the EXTENSIVE TEST is the CHIP HEAT MODE, which is designed to raise the module's temperature. The FINAL TEST portion of the EXTENSIVE TEST will then test the 'heated' module to determine if any speed drift or other temperature related problems have occurred.

The AUTO-LOOP test follows the EXTENSIVE test. This test will continuously test the module with different patterns of data bits.

```
 AUTO-LOOP TEST
LOOP#1090          B2
00:37:51.9  51/100nS
2Mx32     5.25V  FPM
```

The AUTO-LOOP test will terminate only when an error is encountered, or when the user intervenes and stops the test manually. Therefore, the AUTO-LOOP test provides you with perfect BURN-IN capabilities.

The SINGLE BIT test allows you to test each individual data bit of the module by itself with minimal interference from other data bits. Only the actual RASx and CASx control lines, which connect to the currently tested bit, are activated. The Access Time of each bit and its associated control lines are displayed progressively as each bit is tested. The SINGLE BIT test is mostly used for repairs or for detailed quality control analysis. For example, this test is useful when a common error is detected during BASIC test (for example, an address line error) and you want to isolate the error to individual chip/s.