APPENDIX D:

EDO/FPM TIMING MEASUREMENTS

The most important parameter of a memory chip is its speed capability, which is characterized by its Access Time. The Access Time is the dominant factor in the cost of memory chips and modules. It is also the only parameter, which is marked on the chips.

The primary function of a memory chip is to retrieve and to store data. Ideally, it would be very desirable if a memory chip could deliver its stored data at the exact instant of time when it receives the read command. In practice, this process does take some length of time, which is generally called Access Time. Intuitively, the Access Time of a memory chip is the length of time from the moment the chip is instructed to read specific data until the point in time when the required data is available at the chip's output.

DRAM chips utilize a clever accessing scheme which allows them to address 16,000,000 cells (which require 24 address bits) by scanning the address bits in two portions (ROW and COLUMN). As a result, a 16M chip can use only 12 pins for the address bits. To load the address, two control signals, RAS (Row Address Scan) and CAS (Column Address Scan), are applied sequentially to the chip. The period of time between the initiation of the RAS signal until the instant when the data is available at the chip's output is called the DRAM Access Time. The Access Time determines the speed of a memory chip: A chip with a shorter Access Time is faster.

The chip manufacturer marks (and rates) chips with the WORST CASE condition. In other words, the manufacturer fully guarantees that the chip Access Time will either meet or exceed its marked rating under full-recommended operating conditions. The industry standard "recommended operating conditions" means operating voltages from 4.5V to 5.5V, temperature from 0^{o}C to 70^{o}C, maximum capacitance load on the data-line of 100pF, and maximum data-line load of 2 TTL input loads.

RAMCHECK measures the ACTUAL Access Time of the chip as it is subjected to the maximum recommended loading condition and under the lowest voltage within the chip specifications.

You will be surprised to see that in most cases the ACTUAL Access Time is much better than the manufacturer's rating because most manufacturers tend to have a substantial margin of safety. However, as the DRAM technology matures (namely, chips with faster ratings), the difference between the manufacturer's rating and the ACTUAL Access Time becomes smaller: a typical 150nS rated chip may have 100nS ACTUAL Access Time at room temperature, while an 80nS rated chip may have 70nS ACTUAL Access Time at room temperature.

While RAMCHECK helps you to sort out faster memory modules in comparison to their marked WORST-CASE Access Time, care should be taken along the following general guidelines:

1. Memory chips become slower at higher temperatures - the same chip, which can run at 54nS at 25^{o}C, may slow down to 68nS at 70^{o}C. Therefore, the BASIC RAMCHECK test which is conducted at room temperature may show a better Access Time than the later EXTENSIVE test that includes the Chip-Heat mode, where the module will actually be warmed to true working temperatures.

2. Memory chips become slower at lower voltages - the same chip, which can run at 90nS at 5.5V, may slow down to 100nS at 4.5V. Therefore, RAMCHECK's Access Time tests are conducted at 4.5V for 5.0V devices and at 3.0V for 3.3V devices.

3. Other speed related factors (e.g. loading conditions) may be different in your particular application as compared to the testing conditions.

After obtaining the speed of the memory module from your RAMCHECK, determine your own margin of speed-variation and base it on the above arguments and your particular application. Experiment with modules of different actual Access Times to determine your margin of safety. We would like to emphasize that RAMCHECK provides you with the ACTUAL Access Time reading, with no added artificial margin.

With RAMCHECK, the actual Access Time is automatically calculated and displayed. There is no need to set an Access Time switch. The module's Access Time is determined by the slowest chip on the module. Additionally, the Chip-Heat mode warms the module to actual working temperatures, an important parameter in Access Time measurement.

Cycle Time Measurement

One of the unique achievements of RAMCHECK is the ability to test the cycle time of the memory device. It is important to understand the difference between a module's cycle time and its access time. The *access time* of a memory device is the minimum time delay between the initiation of the access operation and the time when the accessed data is available at the device output port. The access time is the timing parameter marked on the memory chip and is readily tested by RAMCHECK. The *cycle time* of the memory device is the minimum time delay from one memory access to the next. Therefore, the shorter the cycle time, the more data accesses can be performed each second (higher data rate). After each access, the DRAM device needs a time-out period (called a precharge time). This precharge time significantly slows down the cycle time of DRAM devices and therefore becomes a speed-limiting factor in DRAM operation. RAMCHECK's ability to test cycle time is an important feature not previously available on comparable testers. This enhances the usefulness of RAMCHECK in determining the quality and actual operational speed of the tested memory devices.

APPENDIX E:

MODULE REPAIR WITH RAMCHECK

RAMCHECK is not merely a Pass/Fail tester. It is designed to provide you with explicit error data to enable you to identify the defective component/s on the DUT.

The RAMCHECK test starts first by checking the external wiring of the DUT, then it quickly determines the structure and speed of the DUT and identifies internal wiring problems, DRAM modes (e.g. EDO), and any defective DRAM interface circuitry. After this set of quick tests, the entire memory array is thoroughly examined.

You will find the following features to be useful in your repair efforts:

1. *The Test Log:* All the test results, structure/speed information and detected errors are reported on the screen and immediately stored in the Test Log. The Test Log is accessed from STANDBY mode by pressing F4 and it contains all the information from the last test. Upon exiting the Test Log, all error menus are re-created; allowing you to extract any information you may have missed during the actual test. Even if the test is prematurely terminated once an error is detected, you can still find valuable information in the Test Log.

2. *Continuation After Error:* RAMCHECK does not stop when it encounter errors, unless the error is FATAL in nature (like "RAS0 stuck at 0" which will terminate the test as you cannot access the DUT). You can continue to test after most error messages by pressing F1. This gives you more information as can be shown in the following example. Suppose RAMCHECK first halts the test with an address error. If you continue the test, a data bit error may further indicate which chip/s caused the error (unless, of course, the address error is due to a connector problem common to all the chips).

3. *Advanced Setup:* You may also use the advanced setup features outlined in Section 5 to further analyze the errors. Such setup features allow you; for example, to test only part of the DUT (setup size) or you can fix the speed at much slower values. You can also check the device at specific values for Trcd, Trah, and other parameters.

RAMCHECK's errors generally identify the relevant pins (circuit connections to the test socket) of the DUT which are associated with the problem. You can remove the DUT from the socket and review the Test Log, which is kept in RAMCHECK's own memory, until you start another test.

Only a technician with component-level repair expertise can repair a memory module. The required soldering/desoldering equipment is relatively complex, especially with modules and cards made with extremely thin Surface Mount technology (i.e. devices with TSOP chips). Nevertheless, a few minor problems, which are identified by RAMCHECK, can be repaired with simple tools. A short between an adjacent pin may be caused by a small piece of metallic debris, which is stuck between two chips. You "repair" the module in this case with an Exacto knife or a watchmaker's fine screwdriver by simply removing the debris.

If you use RAMCHECK in the production shop, you should be able to easily replace the DUT's components. You will need to convert RAMCHECK's error notifications from pin numbers to the actual parts on your DUT.

When working with 72-pin SIMM modules or 168-pin DIMMs, you will need to have a wiring diagram of the module to identify the chip which is connected to the data line (DQ pin) which was identified as bad by RAMCHECK. Module wiring diagrams and DRAM chip data sheets are available from their manufacturers.

If you do not have the actual wiring for the DUT, do not despair. With hundreds of DUT board designs available, wiring diagrams may be hard to find. You can, however, use a continuity meter from the pin identified by RAMCHECK to find the connected chip. Please note that with data (DQ) type error, you can identify the actual defective chip, taking care to work on the DUT's BANK (B1, B2, etc.) identified by RAMCHECK. If the problem is with address lines that are common to all chips, you may need to run more tests (press F1 to Continue when the address error is first reported). Of course, if the address line problem is on the trace to the DUT's connector, the address error is common to all chips.

If you work with the older 30 pin SIMMs, identification is typically easier. For example, if the module is made up of 8 or 9 chips, bit 1 is in the chip closest to pin 1 of the module. Bit 2 is the second chip and so forth. If the module is made with three chips, then bits 1 to 4 are in the left chip (the one closest to pin 1), and bits 5 to 8 are in the middle chip. Bit 9 is in the furthest right chip.

APPENDIX F:

MEMORY MODULE TECHNICAL REVIEW

Throughout the computer era, the need for faster and denser memory devices has put constant pressure on memory manufacturers. The push to maximize memory capabilities has resulted in ever-changing technology.

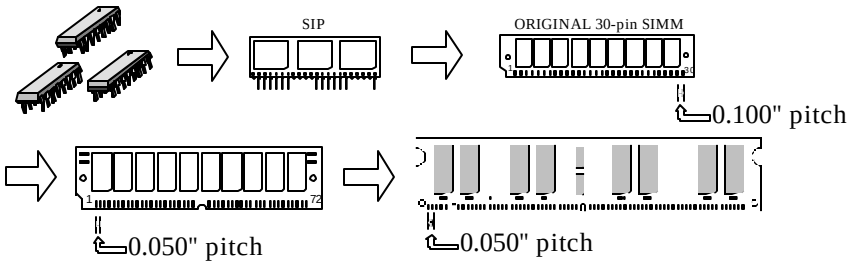
The Evolution of the DIMM Module

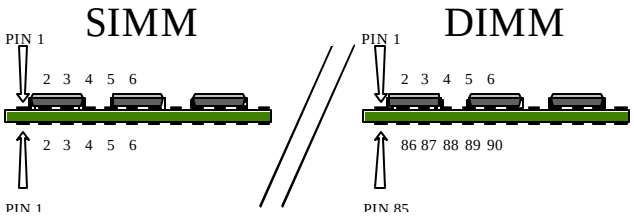
In the early and mid-80s, memory modules were made in a variety of pinouts and without any dominant standards. Early PCs used individual DRAM chips on the motherboard. An early module, the TM4164EQ5 had five such chips on a 24-pin module to achieve a 64Kx5 module.

The first 22-pin SIP (Single Inline Package) modules appeared in the early 80s, comprised of memory devices mounted on a PCB with 22 interconnection pins spaced at 0.100" intervals along a line. Memory modules became popular only after the Wang Laboratories invention of the SIMM (Single Inline Memory Module) technology, where the SIP's legs have been replaced by an edge connector and a convenient mounting feature which includes a special tab to identify pin 1 and two mounting holes.

By the early 90s, most computer systems switched to the SIMM technology due to greater space saving capabilities. Original SIMMs had 30 contacts (pins) which were spaced apart at 0.100". Although contacts for the SIMM device appear on both sides of the edge connector, all opposite contacts are shorted together across the board to achieve more reliable contact with the SIMM socket (see illustration). With the 30-pin limited to 16Mx9, IBM extended the SIMM pin count to 72 for their PS/2 computers, thus allowing for modules with 16Mx36 or x40 bits. To make the PS/2 SIMM module small, the spacing between the contacts was halved to 0.050", but opposite contacts were still shorted across the edge connector.

All solid state memory configurations are now coordinated and standardized by the Electronic Industries Association through its JEDEC Standard 21-C.





The emergence of 64-bit Pentiums triggered the need for modules with a data bus supporting at least 64 bits. The 72-pin SIMM did not have enough pins to accommodate such a wide bus since many additional pins are required for the address, control and power connections. As a result, the DIMM (Dual Inline Memory Module) originated. Improvements in socket technology assured reliable contacts on both sides of the edge connector. The advent of DIMMs made use of these contacts, in effect doubling the connection density of the SIMM.

The first DIMM devices were the 72-pin DIMMs and the 168-pin DIMMs. The 72-pin DIMM is intended for mere size reduction of a 72-pin SIMM for use in portable computers. The 168-pin DIMMs allow for 64-80 bits configuration, and are used for both Standard DRAM and Synchronous DRAM (SDRAM) modules. Recently added is the 144-pin DIMM, with more configurations to be expected.

The following is the pinout of the 168-pin DIMM modules.

Pin No.	Pin Name		Pin No.	Pin Name		Pin No.	Pin Name
1	GND		61	NC		124	Vcc
2-5	DQ0-3		62	Vref/NC		125	Clk1/NC
6	Vcc		63	ClkE1/NC		126	A12/B0
7-11	DQ4-8		64	GND/NC		127	GND
12	GND		65-67	DQ25-27		128	ClkE0/NC
13-17	DQ9-13		68	GND		129	-RAS3
18	Vcc		69-72	DQ28-31		130	-CAS5
19-22	DQ14-17		73	Vcc		131	-CAS7
23	GND		74-77	DQ32-35		132	A13/PDE
24-25	Chk Bit		78	GND		133	Vcc
26	Vcc		79	Clk2/PD1		134	Chk Bit
27	-WE0		80	NC/PD3		135	Chk Bit
28	-CAS0		81	NC/PD5		136-137	DQ54-55
29	-CAS2		82	SDA/PD7		138	GND
30	-RAS0		83	SCL/IDO		139-142	DQ56-59
31	-OE0		84	Vcc		143	Vcc
32	GND		85	GND		144	DQ60
33-38	A0,2,4,6,8,10		86-89	DQ36-39		145	NC
39	BA1/A12		90	Vcc		146	Vref/NC
40	Vcc		91-95	DQ40-44		147	NC
41	Vcc/NC		96	GND		148	GND/NC
42	Clk0/NC		97-101	DQ45-49		149-151	DQ61-63
43	GND		102	Vcc		152	GND
44	-OE2		103-106	DQ50-53		153-156	DQ64-67
45	-RAS2		107	GND		157	Vcc
46	-CAS4		108	Chk Bit		158-161	DQ68-71
47	-CAS6		109	Chk Bit		162	GND
48	-WE2		110	Vcc		163	Clk3/PD2
49	Vcc		111	-CAS/NC		164	NC/PD4
50	Chk Bit		112	-CAS1		165	SA0/PD6
51	Chk Bit		113	-CAS3		166	SA1/PD8
52-53	DQ18-19		114	-RAS1		167	SA2/ID1
54	GND		115	-RAS/NC		168	Vcc
55-58	DQ20-23		116	GND			
59	Vcc		117-122	A1,3,5,7,9,11			
60	DQ24		123	A13			

Memory chips are internally arranged in a ROW/COLUMN matrix selection (actual architectures are somewhat more complex but conceptually the same). -RAS is used to strobe the ROW address lines and -CAS is used to strobe the COLUMN address. As a result, only 11 address lines are needed to create the real address of 22 bits required for 4Meg modules. DRAM memory chips operate in accordance with a variety of protocols (namely, the order of –RAS, -W, and -CAS and other control signals). Interested readers should refer to memory data sheets for more details. RAMCHECK has full software control of all the module pins and it can test the behavior of the module under most possible protocols.

SDRAM modules employ –S signals in place of –RAS control lines, while the DQMB signals replace the –CAS lines.

True 3.3V Testing

The overall trend toward 3.3V was initially inspired by the goal of reducing power. In complex devices like CPUs and DRAMs, the shrinking geometry of the manufacturing process creates an unwanted large electrical field between silicon regions of opposite charges which may break the thin dielectric isolation layers. Reducing the main voltage to 3.3V shrinks these electrical fields thus allowing for smaller geometry and higher DRAM densities. RAMCHECK includes special circuitry to perform true 3.3V testing, which means that all signals to the DUT (device under test) are set within the 3.3V range, not just the power supply. Voltage tests change the voltages to the range of 3.0V-3.6V.

APPENDIX G:

RAMCHECK EXPANSION PORT

RAMCHECK's design allows ample room for expansion and enhancement using its expansion ports. In addition to standard adapters, we design customized adapters for customers' proprietary modules. Alternatively, we can also support customers in their in-house development of their own special adapters.

The most effective way to design a customized adapter for testing non- standard memory devices is to connect the adapter directly to the expansion ports of RAMCHECK. This socket has 40 data lines (DQ type), 16 address lines, 4 RAS lines, 4 CAS lines, two write lines, four PRD lines, numerous power lines, and several special purpose lines.

These ports provide a more than adequate means for testing DIMMs with up to 80 data lines, 8 CAS lines, 2 Id lines and 8 PRD lines.

Please contact us for more detailed examination of your specific requirements.

APPENDIX H:

RAMCHECK MAINTENANCE

Please calibrate periodically. Factory calibration at regular intervals keeps your unit current to existing specifications.

H.1 SYSTEM CALIBRATION

Please refer to our website regarding information on system calibration for your RAMCHECK unit.

H.2 RAMCHECK INTERNAL ARCHITECTURE

Referring to Figure 1, RAMCHECK is made up of two PCBs joined together through a 96-pin connector. RAMCHECK can be opened by removing the six anti-skid rubber feet, then removing the six corresponding phillips screws from the bottom of the enclosure. Once these screws are removed, you can simply lift up the top shell, as shown in Figure 1. The RAMCHECK keyboard and the 128x32-pixel LCD board are attached to the lower PCB (also known as the Processor Board) using solderless connectors and screws. The top board, known as the DIMM Board, can be detached at the 96-pin connector on the left.

H.3 Replacement of 168 pin socket

The socket used by RAMCHECK is attached to the internal PCB with the use of solderless pin receptacles, or barrel sockets. Therefore, socket replacement is almost effortless, as no desoldering is required.

Socket Removal

1. Referring to Figure 1, remove the (6) anti-skid rubber feet, then the screws (#4x3/8 machine phillips).

2. Separate the case halves to expose the circuit boards.

3. Remove the (6) retaining screws (4/40 x 5/16 phillips) from the top circuit board. Pull top circuit board straight up, separating it from the bottom board at the 96-pin connector on the left as shown in Figure 2**.**

4. Remove the (2) screws (4/40 x 7/16 Slot Pan Head) on either side of the 168-pin socket**.**

5. Gently, using a rocking motion, pull to separate the socket

from the circuit board.

Socket Insertion

1. Assure that there is no debris in the area where the new socket is to be placed.

2. Align the pins of the socket with the barrel sockets and gently push the socket into the PC Board.

3. Replace (2) screws (4/40 x 7/16 Slot Pan Head and tighten (Avoid damaging the circuit board by over tightening). See Figure 2**.**

4. Replace the top circuit board and replace (6) screws (4/40 x 5/16 Phillips) and washers (do not over tighten)**.**

5. Place the case halves back together and replace (6) screws (#4 x 3/8 machine Phillips), do not over tighten. Replace the rubber feet**.**

Refer to Section 3.3 for additional information on adjusting the LCD.

H.4 CHANGING JUMPER SETTINGS

Figure 4 illustrates the jumpers on the RAMCHECK's processor board. These jumpers are setup at the factory, therefore you will rarely need to modify them. You will not need to change JP1 and JP7 as they are used for board testing only.
JP6 controls the intensity of the LCD backlighting. It is set by default for LOW backlight, however, if you wish to switch to HIGH backlight, you may set JP6 to the upper most settings.

JP5 controls the size of the SRAM chips installed in your board, which is currently 64KB SRAM. There may come a point when RAMCHECK's SRAM chips will be upgraded to 128KB or 256KB, which requires setting the JP5 jumper to the left.

FIGURE 1
RAMCHECK INTERNAL ARCHITECTURE

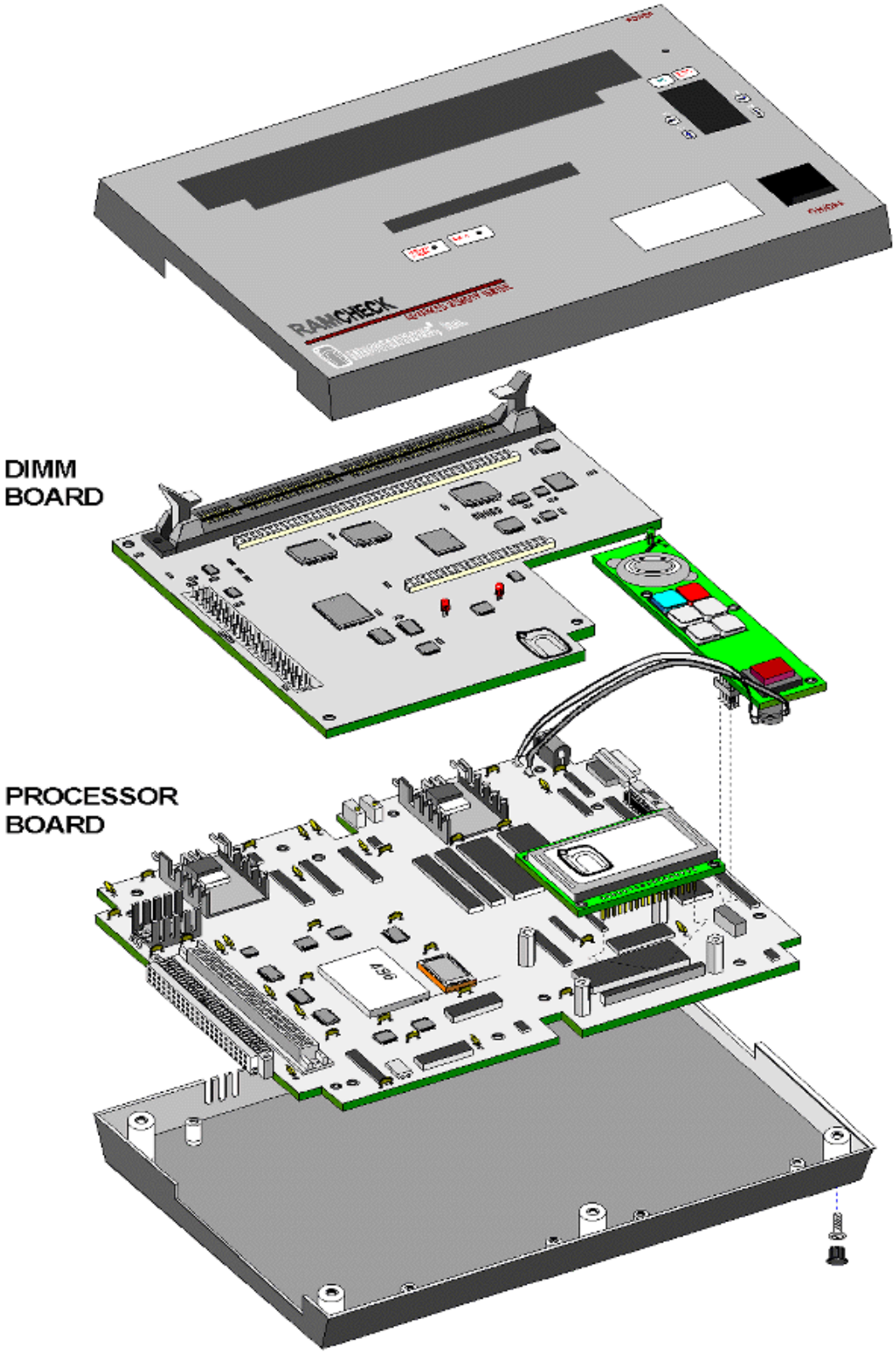


FIGURE 2

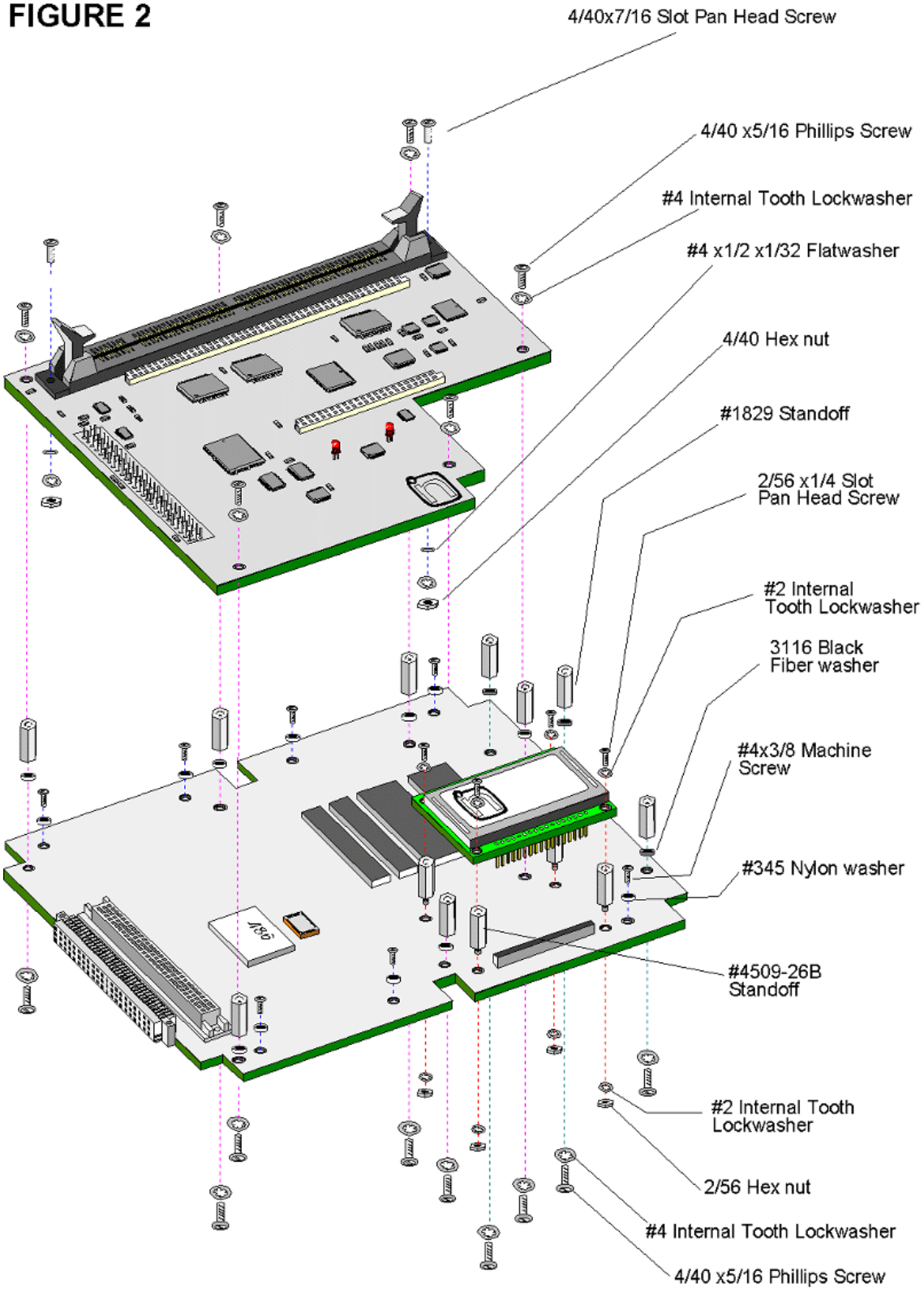

4/40x7/16 Slot Pan Head Screw
4/40 x5/16 Phillips Screw
#4 Internal Tooth Lockwasher
#4 x1/2 x1/32 Flatwasher
4/40 Hex nut
#1829 Standoff
2/56 x1/4 Slot Pan Head Screw
#2 Internal Tooth Lockwasher
3116 Black Fiber washer
#4x3/8 Machine Screw
#345 Nylon washer
#4509-26B Standoff
#2 Internal Tooth Lockwasher
2/56 Hex nut
#4 Internal Tooth Lockwasher
4/40 x5/16 Phillips Screw

FIGURE 3

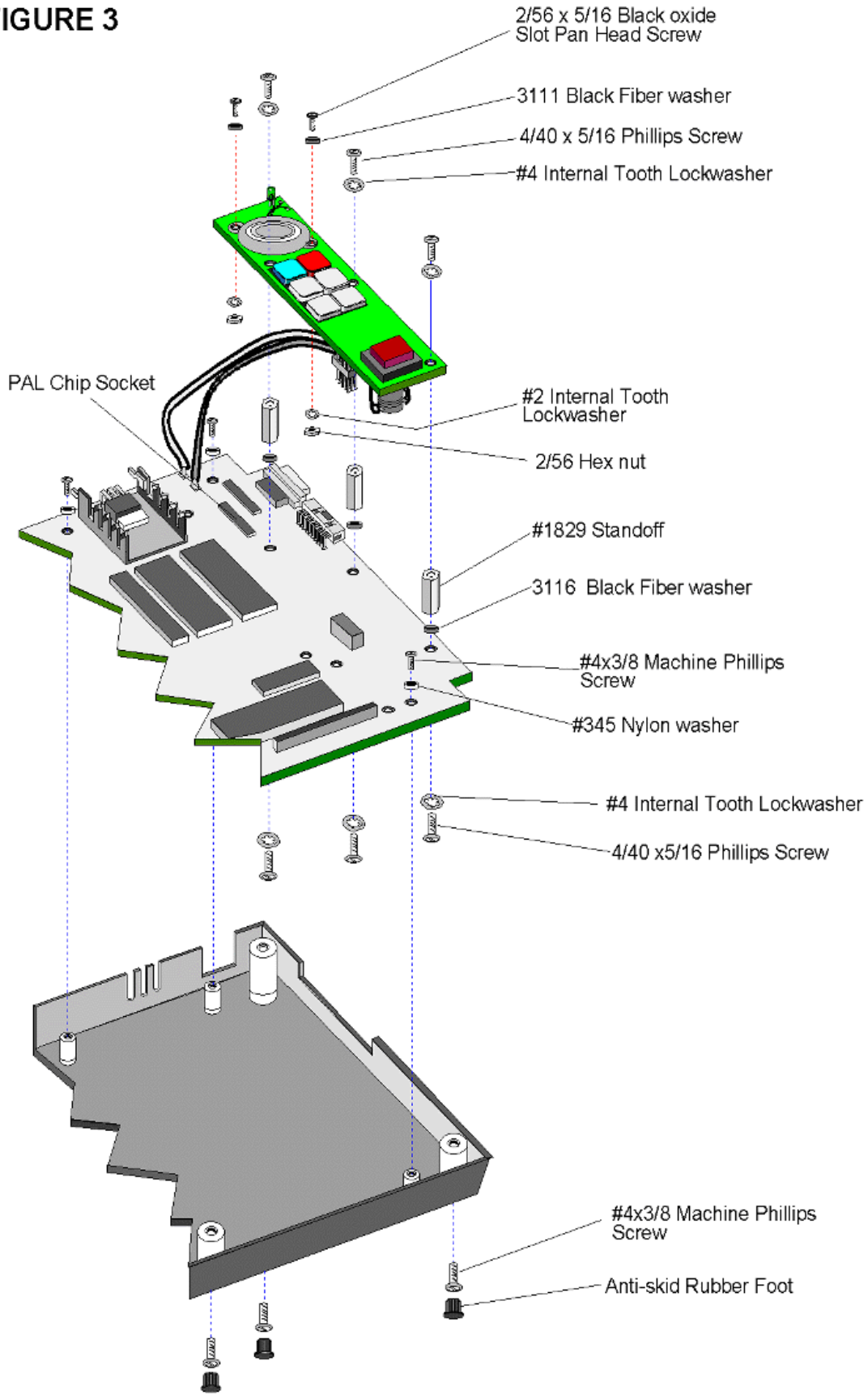
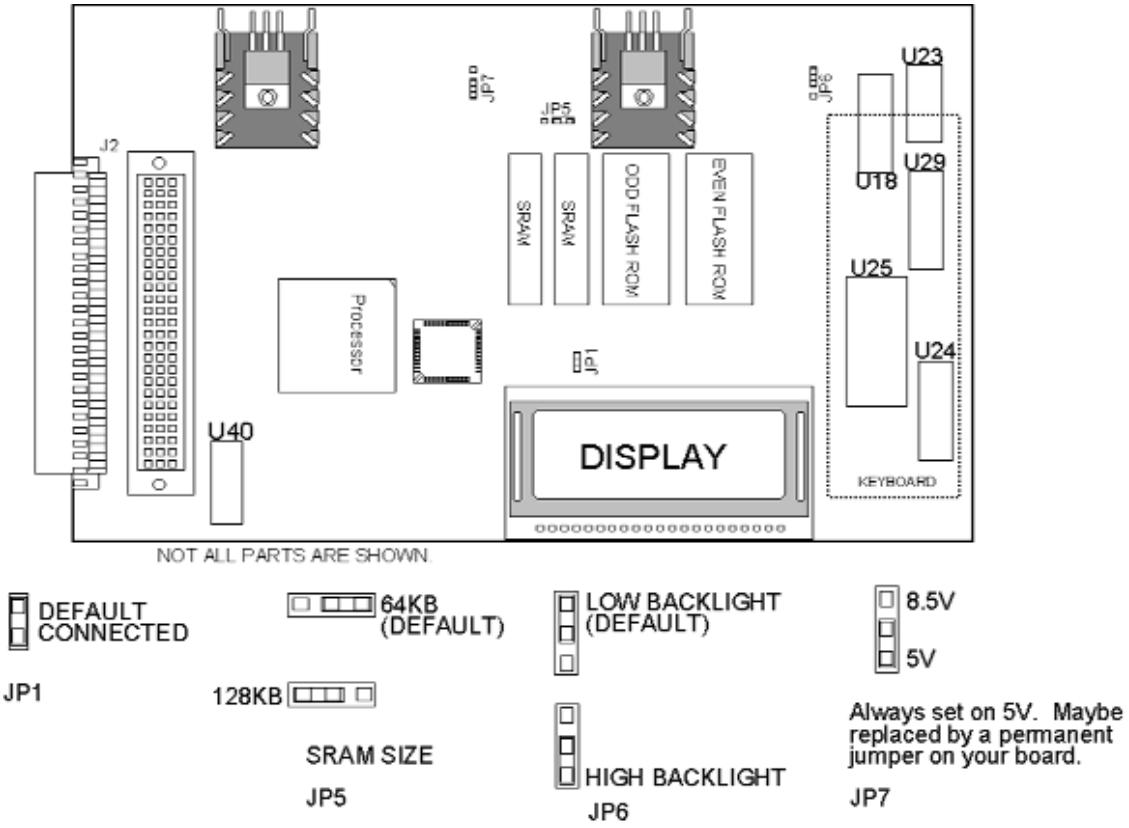

2/56 x 5/16 Black oxide
Slot Pan Head Screw
3111 Black Fiber washer
4/40 x 5/16 Phillips Screw
#4 Internal Tooth Lockwasher
PAL Chip Socket
#2 Internal Tooth
Lockwasher
2/56 Hex nut
#1829 Standoff
3116 Black Fiber washer
#4x3/8 Machine Phillips
Screw
#345 Nylon washer
#4 Internal Tooth Lockwasher
4/40 x5/16 Phillips Screw
#4x3/8 Machine Phillips
Screw
Anti-skid Rubber Foot

FIGURE 4



Refer to Section 7.5 for additional information on the Direct Printer Interface.

H.5 PRINTER PAL CHIP

RAMCHECK comes with a 16-pin IDC connector to support the optional Direct Printer Interface. This IDC connector is controlled by the special PAL chip that comes with your Direct Printer Interface. This section explains how to install this PAL chip into the designated socket inside RAMCHECK (see Figure 3).

You must first remove the six rubber feet and their corresponding phillips screws from the bottom of the RAMCHECK enclosure (Refer to Figure 1). This will allow it to be separated and reveal RAMCHECK's internal architecture.

The socket U18 for the PAL chip is located underneath the RAMCHECK KEYBOARD. Remove the three 4/40 x 5/16 phillips screws from the keyboard (Figure 3) and gently disconnect the keyboard from the Processor Board (the bottom PCB of RAMCHECK).

Install the special PAL chip that is enclosed with your

RAMCHECK Adapter into the empty socket marked U18 (See Figure 3) located just below the electrolytic capacitors on the Processor Board.

Reconnect the keyboard to the Processor Board and secure it with the three phillips screws. Close the RAMCHECK unit and test your installation with your Direct Printer Interface.

APPENDIX I:

SPECIFICATIONS

General: RAMCHECK (p/n INN-8668) tests 168-pin SDRAM/EDO/FPM DIMM modules. For further information on keeping your system up to current factory specifications, please visit our Calibration and Hardware Upgrade page.

Internal Construction: Three Printed Circuit Boards connected with a 96-pin snap-on connector.

Chip technology: Advanced CMOS and FCT devices.

Processors:
Main Processor: TX486DLC/E-40GA running at 40MHz Max.
Secondary processor (SDRAM test engine): ALTERA CPLD running at 184MHz Max.

Internal SRAM: 64KB (Expandable to 256KB).

Internal SDRAM: 6MB.

Internal Program FLASH EPROM: 512KB (Expandable to 1MB). Internal Program can be upgraded via the Internet.

PC Interface: Built-in Serial Interface (9-pin connection cable is included). RAMCHECK is a stand-alone tester. PC Communications software is included to provide printed reports, data logging, and firmware upgrades via the Internet.

Display: Standard 128 x 32 pixel LCD (Reflective) with LED backlighting and 6 o'clock view direction (internal contrast control located on bottom PCB).

DUT (Device Under Test) interface:
16 multiplex DRAM/MODULE address lines for up to 4G addresses of direct processor access
Main Control lines: 4 -RAS/-S lines, 8 -CAS/DQM lines, 2 –W/WE lines, 2 -OE lines, 2 CKE and 4 Clock lines (for SDRAM only).
Complex wave generation and digital delay synthesis on all -RAS/-S, -CAS/DQM and -W lines.
Advanced setup of Trcd and Trah setup at 1-2 nS resolution.
Three Programmable Regulated Voltage Sources 1.25V-5.7V with automatic current limiters.

EDO/FPM DRAM Access Time: Direct measurement from 150nS down to 20nS at 1nS resolution, +/-3nS accuracy.
SDRAM Clock Access Time: Direct measurement from 150MHz to 66MHz with 0.5nS resolution, +/-1nS accuracy.

TEST ALGORITHM:
Checker Patterns.
Walking 0, 1.
Voltage Cycling and Voltage Bounce.
March Up/Down.
Self-Refresh (for SDRAM).
Auto-Loop with changing patterns.

AC LINE ADAPTER: Universal Power Supply, UL/CSA listed 100-250VAC/47-63Hz to 7.5VDC @ 4 AMP adapter.

Dimensions: 9.5" x 6.5" x 3" (W x L x H).

NET Weight: 3.5 lbs.

Shipping Weight: 10 lbs.

PROBLEM REPORT FORM

Please contact us regarding any service that is needed by your equipment. Please do not send any package to us unless you have been authorized by our tech department and have been issued an RMA number. After receiving authorization, be sure to include this form along with your merchandise and be sure to be as descriptive as possible when discussing the problem you are experiencing. Please duplicate this form if you need additional copies. We will review your comments promp tly and contact you if necessary.

Name: _____ Title/Dept: _____

Company: _____

Address: _____

City: _____ State: _____ Zip: _____

Phone: _____ Ext: _____ FAX: _____

Return Merchandise Authorization (RMA) #: _____

Program Version (as seen on entry screen): _____

Type of module tested (DIMM, CHIP, Size, Manufacturer, etc.):

_____

Problem Description:

_____

_____

_____

_____

_____

_____

To be Completed by INNOVENTIONS:

PRF#_____Received:_____ Engineer:_____