APPENDIX A:

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APPENDIX B:

SIMCHECK II TEST ALGORITHMS

SIMCHECK II's proprietary test algorithms were developed for optimum efficiency and fast testing. SIMCHECK II utilizes different patterns and different algorithm types whenever the same module is re-tested. Tests are of type O(n), using MARCH, CHECKER, WALKING 0s, WALKING 1s and Surround Disturb Patterns.

The complexity of testing a memory chip can be understood from the following example: let us assume that we want to test a simple hypothetical memory chip of only 8 cells. A simple approach is to first write "0" in all the cells and verify that the cells hold the data, and then write "1" in all the cells and verify. Thus in only 16 write/read cycles we have "completely checked" this chip. **However, there is a major flaw** in this conclusion since it is possible that cell number 2 is shorting (or otherwise disturbing) cell 7, and the above test will not detect this!

An alternate approach is to exhaustively test the memory with all possible combination of "0"s and "1"s in all the cells. First we write and verify with all "0"s. Second, we write and verify with "1" in cell 1 and "0"s in all other cells. The third test checks cell 2 with "1", "0"s in all others, etc. Overall, we need to test this hypothetical chip with 2^8=256 patterns, since each pattern has at least 8 write/read accesses to the chip. Based on the example above, it will take at least [256,000 x $2^{256,000}$] accesses to fully test a 256K memory chip. This number is astronomical - and therefore it is theoretically impossible to create a test for a modern memory chip with 100% accuracy.

Fortunately, most inter-cell disturbances in a memory chip occur between adjacent cells, so that a fully exhaustive test as mentioned above is not required.

During the years since our RAMCHECK and SIMCHECK line of products were first developed, the test algorithms have been continuously improved to achieve unparalleled accuracy in testing memory chips. The proprietary programs, which have been thoroughly tested and refined in RAMCHECK and SIMCHECK, have been transported to SIMCHECK II and have been further improved. For example, using programmable voltage sources, our test algorithms use advanced tests incorporating Voltage Bounce and Voltage Cycling. The first provides higher accuracy in detecting pattern sensitivity and other intermittent memory problems. The latter provides additional assurance of proper product operation under the entire manufacturer's voltage specifications. Another addition is our Chip-Heat mode, which warms the tested module to true working temperatures, thereby improving the reliability of temperature related measurements. So despite the complexities enumerated above, your SIMCHECK II can trap most defective memory modules.

APPENDIX C:

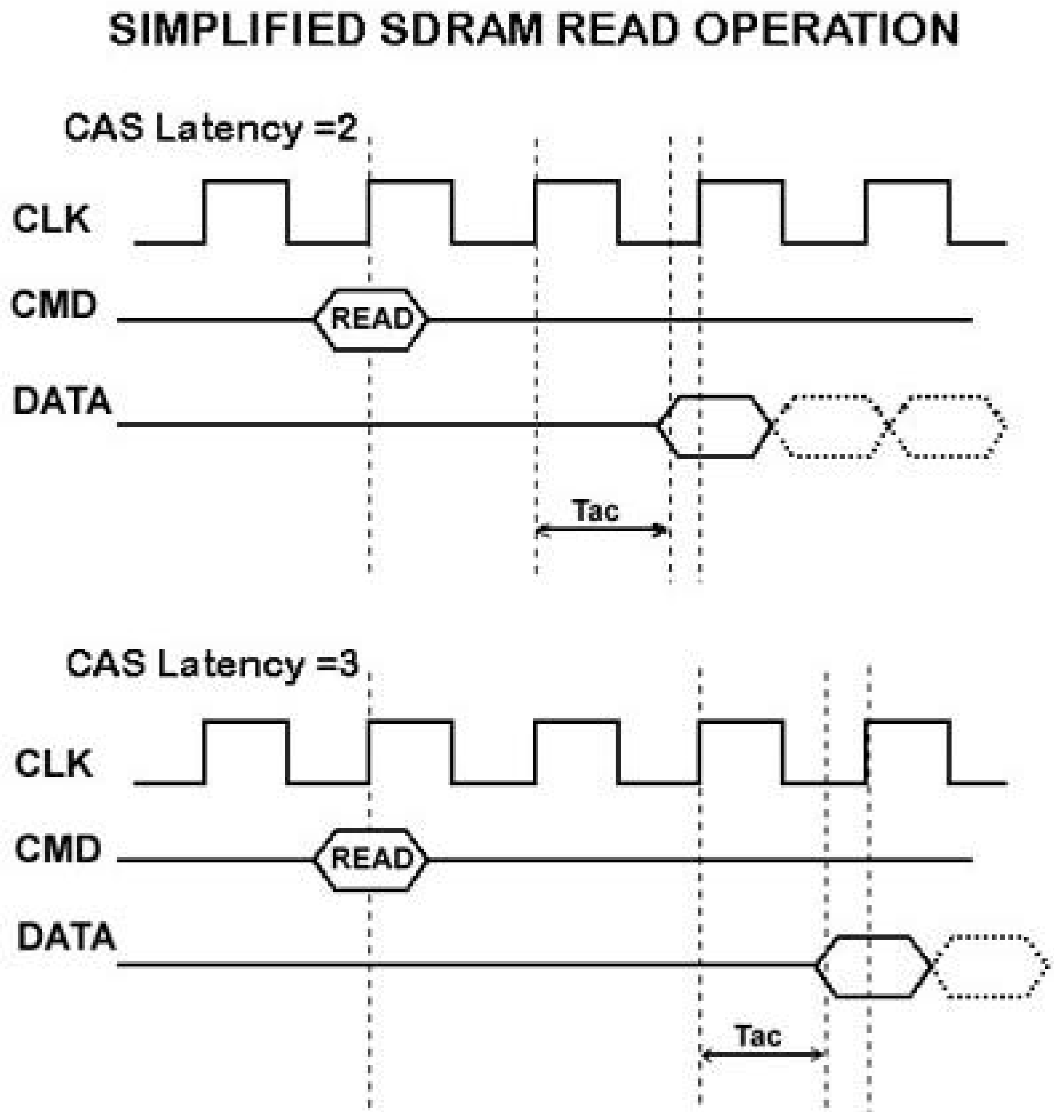
SDRAM TIMING AND PC-100/PC-133 COMPLIANCE

The Access Time from Clock (Tac) is one of the important timing parameters of the SDRAM memory device and it is critical for PC-100 and PC-133 compliance. This application note explains the Tac timing parameter, illustrates its dependency on CAS Latency 2 or 3, and explains how the Sync DIMMCHECK measurement of this parameter is used to interpret compliance with the PC-133/PC-100/PC-66 standards.

Access Time From Clock (Tac)

The access time from the clock signal (Tac) is dependent on the CAS Latency setup. For CAS Latency 3, first data is valid at the rising edge of the third clock from the read command. For CAS Latency 2, first data is valid at the rising edge of the second clock from the read command. The following drawing illustrates the CAS Latency in a simplified way. It is assumed that the bank ACTIVE command, which is needed to start any SDRAM activity, has been properly initiated prior to the READ command. The read data can be a burst of 1, 2, 4, 8, or even a full page of data, depending on the SDRAM setup. Therefore, CAS Latency determines when the first data is valid.

As shown in the drawing, for CAS Latency 2, the Tac parameter is the time from the rising edge of the first clock after the READ command to the time that first data is valid. For CAS Latency 3, the Tac parameter is the time from the rising edge of the second clock after the READ command to the time that first data is valid. The access time from clock is also called Output Valid From Clock.



INTEL PC-100/PC-66 Tac Limits

Intel specifies the following limits for the Tac parameter:

Output Valid From Clock (Tac)	PC-66	PC-100
CAS Latency=2 Limited Application	10.0 nS	7.0 nS
CAS Latency=2 Full Application	9.0 nS	6.0 nS
CAS Latency=3 Full Application	9.0 nS	6.0 nS

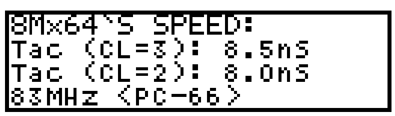
Intel specs acquired from the Intel Serial Presence Detect Specification revision 1.2A; further information can be acquired by visiting:
http://developer.intel.com/design/pcisets/memory/index.htm.

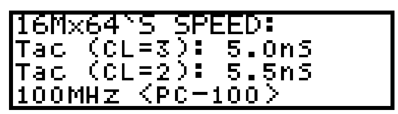
PC-133 Tac Limits

The PC-133 is essentially based on the INTEL PC-100 specification with the enhancement of 133MHz operation at a CAS Latency of 3 (CL=3) and access time from clock (Tac) of 5.4nS. Accordingly, the SPD data of a PC133 module is similar to the PC-100 SPD data, with the exception of byte 9 (SDRAM device cycle time CL=3) set to 75h (7.5nS) and byte 10 (SDRAM device access time from clock at CL=3) set to 54h (5.4nS).

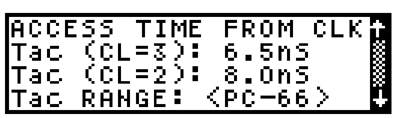
Sync DIMMCHECK Tac Measurements

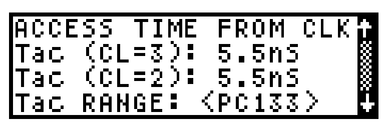
At the start of the Basic test, SIMCHECK II measures the module's Tac at CAS Latencies of two and three. If the module has two banks, SIMCHECK takes the slower measurements (higher access time in nS) into account. The program uses specific margins to determine if the tested module exhibits Tac in the range of the PC-133, the PC-100 standard or the PC-66 standard. These measurements are shown in the SPEED summary screen at the end of the Basic test (or if you press F5 during Basic test) as follows:





The same data is also recorded in the Test Log as follows:





The SIMCHECK program uses the Tac measurements to determine the test frequency of the module during Basic Test. A module which indicates a Tac Range of <PC-133> will be run at 133MHz, a module with a Tac Range of <PC-100> will be run at 100MHz, and a module having a Tac Range of <PC-66> will be run at 83MHz. Other timing problems of the module may cause it to drift to lower speeds during Basic test or subsequent tests.

Please note that you can still override the speed (using Test Setup or the Change-on-the-Fly feature) to cause a module with a Tac measurement of even 8nS to run at 100MHz, but of course, such a module cannot meet the PC-100 specification of 6nS. Therefore, the fact that a module may run on SIMCHECK at 100MHz or more does not imply that the module is indeed PC-100 compliant.

Some modules which are not certified for PC-133 (and their SPD indicates that they are intended for PC-100) may still score within the <PC-133> range on SIMCHECK, as their access times are indeed quite fast. However, such modules may still exhibit unfavorable results in an actual PC-133 application, as there are several other factors involved in PC-133 compliance. On the same token, some PC-100 modules may slightly miss our margin of accuracy and score within the <PC-66> range.

An exact measurement of Tac requires the use of a very expensive tester with a variable temperature oven, sub-nanosecond accuracy, and complex capabilities to compensate for all loading effects. SIMCHECK II and the Sync DIMMCHECK have an inherent inaccuracy of about +/-1 nS in determining the Tac measurements. Therefore, we are using the notion of Tac RANGE to allow for such measurement inaccuracies and to encourage the user to consider the actual Tac measurements. Other aspects of the SIMCHECK test (some still under development) are further used to determine compliance with the PC-133.

Please note that unlike some of our competitors who measure speed by extrapolating access time measurements while running the modules at very slow clock rates (e.g. 25MHz), Sync DIMMCHECK actually runs the module at the indicated speed. For example, if a module is displayed to run at 133MHz, this is the exact clock rate that the Sync DIMMCHECK provides to the module (you can verify this fact with an oscilloscope connected to the module clock lines). SIMCHECK II and the Sync DIMMCHECK actually measure Tac by averaging a group of measurements done automatically at 80MHz, 96MHz, 100MHz, 112MHz, 125MHz and 133MHz.

Sync DIMMCHECK 168 can determine if a tested module is a PC-133, based on several actual measurements and a smart algorithm that takes into account the actual resolutions of the measurements of our test system.

The algorithm for determining PC-100 compliance uses various measurements made by the tester during the Basic Test. In particular, it uses information from maximum page burst frequency, frequency drift during test, the Tac measurements for CAS Latency 3 and 2, and the SPD data. It also allows for future enhancements when additional measurements will be available as our R&D efforts proceed.

The algorithm for determining PC-133 compliance employs similar methods as for PC-100. However, since the PC133 tests are conducted only on modules that have been detected as "at least" PC-100, a full understanding of our PC-100 determination is essential to understand our PC-133 determination.

The algorithm is a simplified Expert System, as it sometimes needs to judge between conflicting measurements. Therefore, our test summary screens (as well as the Test Log) provide a determination of PC-133/PC-100 compliance AND some of the results that led to that conclusion. Advanced users can further look at the results and determine the margin or accuracy of the SIMCHECK determination.

This section provides the details for our PC-133/PC-100 reports.

NOTATIONS

The following are examples of the first summary screen on SIMCHECK following the end of Basic Test. Alternatively, you can reach this screen even before the end of Basic Test if you abort the test by pressing F5 during Basic Test:

```
8Mx64`S SPEED:  100MHz
TEST=PC-100
PAGE BURST=100MHz
SPD=INTEL PC-100
```

```
8Mx72 SPEED:   133MHz
TEST= PC133 RANGE
PAGE BURST=125MHz
SPD=JEDEC PC133
```

The determination of the PC-133/PC-100 compliance appears on the second line of the screen and it has the header "TEST=" followed by "PC-100" if SIMCHECK determines that the module is PC-100, or “PC-133 RANGE” if SIMCHECK determines that the module is PC-133.

The third line of the first example indicates "PAGE BURST=100MHz" and it indicates that the maximum page burst of the tested module was 100MHz, while the second reached 125MHz. The fourth line of the first example indicates "SPD=INTEL PC-100" which indicates that the data in the SPD claims the module to be a PC-100. The second example indicates the SPD data matches that of a PC-133.

The next example shows the first summary screen of a PC-66 module:

```
2Mx64`S SPEED: 83MHz
TEST=PC-66
PAGE BURST=100MHz
SPD=INTEL PC-66
```

The message "TEST=PC-66" indicates that SIMCHECK has determined that the module is a PC-66. You can see that the bottom line also verifies that the SPD claims the module to be a PC-66.

The third example shows a module that is marked as PC-66 by the SPD, but SIMCHECK determines that the module matches the speed of other PC-100 modules:

```
4Mx72`S SPEED: 100MHz
TEST=PC-100 RANGE
PAGE BURST=112MHz
SPD=INTEL PC-66
```

The message "TEST=PC-100 RANGE" is indicating that the module indeed ran at 100MHz, even though the SPD data shows "SPD=INTEL PC-66". The maximum page burst in this example was 112MHz.

The first summary screen is followed by the Tac measurement screen as in the following examples:

```
8Mx64`S SPEED:
Tac (CL=3): 8.5nS
Tac (CL=2): 8.0nS
83MHz <PC-66>
```

```
16Mx64`S SPEED:
Tac (CL=3): 5.0nS
Tac (CL=2): 5.5nS
100MHz <PC-100>
```

In the case of the PC-133, SIMCHECK first detects that the module under test meets the PC-100 requirements. At that point, the SPD is checked for PC-133 compliance. Afterwards, the fast access time from clock at CL=3 is determined.

If the module can then work at 133MHz, the tester will determine that it is PC-133, showing the speed 133MHz during BASIC TEST and indicating a Tac range of PC-133 during the summary screen and in the test log.

```
16Mx64`S SPEED:
Tac (CL=3): 5.0nS
Tac (CL=2): 5.5nS
Tac RANGE: <PC133>
```

INTERPRETATION OF SIMCHECK RESULTS

An exact measurement and full certification of a module as PC-133 requires the use of a very expensive tester with a variable temperature oven, sub-nanosecond accuracy, and complex capabilities to compensate for all loading effects. SIMCHECK II and the Sync DIMMCHECK have an inherent inaccuracy of about +/-1 nS in determining the Tac measurements. The patent pending page bursting mechanism of the Sync DIMMCHECK provides a fairly accurate measurement of the maximum frequency in which the tested module can burst. By using an Expert System that gives a certain weight for each tested parameter, we are able to provide a close overall determination as to whether the module is PC-133, PC-100, or PC-66. However, 100% accuracy is beyond the scope of this inexpensive tester.

If a PC-133 module is identified as PC-100, or a PC-100 as a PC-66, you can further investigate the measurements and see what margin of error exists.

If a PC-66 module is identified as "PC-100 RANGE", please note the module may or may not work in motherboards that require strict PC-100 compliance. This is why we use the RANGE notation.

IMPORTANT NOTE: The BASIC Test is the only test used by SIMCHECK II to determine compliance for both PC-133 and PC-100 specifications. It provides an information summary that gives specific information if the module is compliant for either of these standards. Other frequencies are used throughout the Extensive Test to create additional conditions for the test. Therefore, if a module finishes BASIC Test as PC-133, the fact that it may run at 100MHz during Extensive Test or AUTO LOOP does not mean that the module is not a PC-133. Similarly, if a PC-100 device runs at 83MHz during the Extensive Test, it still remains a PC-100.